IN THE CLAIMS

Please cancel claim 7 without prejudice, amend claims 2-6, and add new claims 8-14, such that the status of the claims is as follows:

1. (Withdrawn) A low-power-loss power semiconductor switching device comprising an n-type base, a backside p^+ emitter and general frontside structure including a cathode and a gate, wherein said switching device includes a combination of an ultra thin and lightly-doped backside p^+ emitter formed by ion implanting and a nonuniformly doped n-type base which contains a residual layer of a priorly-diffused n^+ layer on one side of the device.

2. (Currently Amended) The method as defined in claim 6 wherein the thickness of the backside p^+ emitter layer is approximately between 0.2 and 1 μm.

3. (Currently Amended) The method as defined in claim 6 wherein the implanting dose of the backside p^+ emitter layer is approximately between $1x10^{11}$ and $1x10^{17}$ cm^{-2}.

4. (Currently Amended) The method as defined in claim 6 wherein the thickness of the n-type residual diffused-layer ~~contained in the n-type base~~ is approximately between 5 and 50 μm.

5. (Currently Amended) The method as defined in claim 6 wherein the doping concentration of the n-type residual diffused-layer is in a range of approximately $1x10^{14}$~$1x10^{17}$ cm^{-3} at the junction interface of the n-type residual diffused-layer and the backside p^+ emitter layer.

6. (Currently Amended) A method for fabricating ~~low-power-loss power semiconductor switching devices~~ IGBT, MCT or GTO, wherein the fabrication is in the following sequence:

PROCEDURE I: from a uniformly-doped monocrystalline n^- starting wafer fabricating a nonuniformly doped n-type substrate which contains ~~a diffused~~ an n^- layer on ~~one side, wherein~~ the frontside of the wafer and a diffused n^+

layer on the backside, wherein the diffused n^+ layer~~, which is finally near to the backside p^+ emitter,~~ is formed in the first step of this procedure ~~before the thinning of the substrate~~;

PROCEDURE II: fabricating the ~~general~~ frontside structure of either an IGBT, MCT, or GTO on the ~~low-concentration side of the n-type substrate using ion implanting, high-temperature diffusion and so on~~ frontside of the substrate whereon the n^- layer is exposed;

PROCEDURE III: thinning the wafer from the ~~high-concentration side~~ backside of the substrate ~~by such commonly used techniques as grinding and polishing, so that the thickness of the residual diffused-layer is decreased to a required value~~, whereon the diffused n^+ layer is exposed, by grinding and polishing, until an n-type residual diffused-layer is reserved;

PROCEDURE IV: forming ~~the~~ a backside p^+ emitter layer ~~with a required thickness~~ by ion implanting into the backside surface of the wafer whereon the residual diffused-layer is exposed thus producing a p-n junction near the backside surface of the wafer which is composed of the p^+ emitter layer and the n-type residual diffused layer;

PROCEDURE V: depositing metals on the backside surface of the wafer whereon the backside p^+ emitter layer is exposed, followed by sintering/alloying; and

after the substrate is thinned, i.e. after finishing PROCEDURE III or since PROCEDURE IV, only low-temperature processes occur at less than 600°C.

7. (Canceled).

8. (New) A low-power-loss power semiconductor switching device formed by the method of claim 6.

9. (New) A method for fabricating a low power loss semiconductor switching device having a voltage rating of less than 2 KV, the method comprising:

diffusing an n^+ layer on a back side of a uniformly doped monocrystalline n^- wafer to form a nonuniformly doped n^- type substrate;

fabricating a frontside structure on a front side of the substrate where an n^- layer is exposed;

thinning the substrate from the back side to expose an n-type residual diffused layer;

forming an p^+ emitter layer by ion implantation on the back side of the substrate on the exposed residual diffused layer;

depositing metals on the back side of the substrate on the p^+ emitter layer; and

sintering and alloying the deposited metals;

wherein the steps of forming, depositing and sintering and alloying occur at low temperatures.

10. (New) The method of claim 9 wherein the low temperatures are temperatures less than 600 °C.

11. (New) The method of claim 9 wherein the step of thinning comprises:

grinding and polishing the n^+ layer of the back side of the wafer to a position determined according to a required voltage rating.

12. (New) The method of claim 9 wherein the low power semiconductor switching device is selected from a group consisting of IGBT, MCT and GTO devices.

13. (New) The method of claim 9 wherein the step of fabricating comprises:

producing the frontside structure using a process selected from a group consisting of ion implantation, high-temperature diffusion, CVD, and evaporation/sputtering.

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14. (New) The method of claim 9 wherein the p+ emitter layer has a thickness between 0.1 and 1 μm.